**Chapter 3 TypeC PHY Electrical Specification**

**3.1 Operating Conditions**

Table 3-1 Operating conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Name | Min | Typ | Max | Units | Description |
| Vavdd\_cmn\_clk | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_h | 1.58 | 1.8 | 1.994 | V | IO supply voltage at the junction. Refer to Table ‘Power supply budget’ |
| Vavdd\_tx\_<> | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_xcvr | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_xcvr\_clk\_<> | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Tj | -40 | 25 | 125 | ℃ | Junction temperature |

Table 3-2 Power supply budgeting

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Name | Voltage | | | | | Description |
| Min | Typ | | | Max |
| Supply Budgeting for avdd and avdd\_clk: 0.9V | | | | | | |
| Off die VRM DC variation | -3.50% | |  | 8.50% | | On board voltage regulator DC accuracy. |
| Off die VRM AC VRM noise | 2.00% | | | | | Peak-to-peak 18mV frequency content: 50KHz to 500KHz |
| 1.00% | | | | | Peak-to-peak 9mV with frequency content: 500KHz to 10MHz; no single frequency noise amplitude can be more than 5mV. |
| Off die total supply variation | -5.0% | | - | 10.0% | | Total off-die voltage variation at package pin of supply die to external voltage regulator. |
| AC Self Induced + Coupling Noise | 1.70% | | | | | This 15.3mV peak-to-peak noise due to switching current through package parasitics. This is wideband. |
| Package IR (DC) drop | -1.0% | | - | 0.00% | | The 9mV IR drop is due to worst case DC current of the PHY. |
| On die IR (DC) drop | -2.50% | | - | 0.00% | | The 22.5mV drop is due to worst case DC current and worst case metal routing parasitic. |
| Final Voltage range (V) | 0.813 | | 0.90 | 1.00 | | This is the expected voltage at the junction. It includes 2.7mV margin for the design. |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Name | Voltage | | | | | Description |
| Min | Typ | | | Max |
| Supply Budgeting for 1.8V IO supply (avdd\_h) | | | | | | |
| Off die VRM DC variation | -8.50% | |  | 8.50% | | On board voltage regulator DC accuracy. |
| Off die VRM AC VRM noise | 2.00% | | | | | Peak-to-peak 36mV frequency content: 50KHz to 500KHz |
| 1.00% | | | | | Peak-to-peak 18mV with frequency content: 500KHz to 10MHz. |
| Off die total supply variation | -10.0% | | - | 10.0% | | Total off-die voltage variation at package pin of supply due to external voltage regulator. |
| AC Self Induced + Coupling Noise | 0.50% | | | | | This 9mV peak-to-peak noise is due to switching current through package parasitics. This is wideband. |
| Package IR (DC) drop | -0.5% | | - | 0.00% | | This 9mV IR drop is due to worst case DC current of the PHY |
| On die IR (DC) drop | -1.00% | | - | 0.00% | | This 18mV drop is due to worst case DC current and worst case metal routing parasitic. |
| Final Voltage range (V) | -1.58 | | 1.8 | 1.994 | | This is the expected voltage at the junction. It includes 0.5mV margin for the design. |

**3.2 Common Electrical Specifications**

3.2.1 Reference Clock Input Specifications

• Minimize exposure to nearby aggressor signals that could contaminate the clock with crosstalk, especially if these signals are lower than 1MHz in frequency.

• If these bumps are not used, it is not necessary to AC couple or terminate these pins. They can be left floating.

Table 3-3 Reference clock specification for USB3 and DP

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Normative Electrical Parameters | Min | Typ | Max | Units | Description |
| External Clock Frequency | - | 24 | - | MHz | - |
| Input Duty Cycle | 48 | - | 52 | % | - |
| Single-ended clock input voltage (CMOS level) | 0.85 | - | 1 | V | - |
| Input Random Jitter | - | - | 140 | dBC/Hz | Noise floor density from 10 KHz to 10 MHz |
| - | - | 2.9 | ps | For a 24MHz  reference,integrated jitter from 10KHz to 10MHz |
| Input determinestic Jitter | - | - | 4 | ps | Over a band of 10KHz to 10MHz |

3.2.2 DP Transmitter electrical specification

Table 3-4 DP Transmitter module electrical Specifications

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Symbol | Description | Min | Typ | Max | Units | Comments |
| UI | UI\_HBR2 | 185.129 | 185 | 186.172 | ps | -Unit Interval for high bit  rate (DP: 5.4Gbps/  lane). Frequency ppm  -5300 to +300 |
| USB3 | 199.94 | 200 | 200.06 | UI with ± 300ppm with-  out SSC |
| UI\_HBR | 370.259 | 370 | 372.343 | Unit Interval for high bit  rate (DP: 2.7Gbps/  lane). Frequency ppm  -5300 to +300 |
| UI\_RBR | 617.098 | 617 | 620.573 | Unit Interval for high bit  rate (DP: 1.62Gbps/  lane). Frequency ppm  -5300 to +300 |
| VTX-DIFFp-p | Differential p-p TX voltage swing  including low power | 100 | - | 1200 | mV | For USB 3.0, no EQ is  required. |
| ITX-SHORT | Transmit lane short-circuit current | - | - | 100 | mA | - |
| RLTX-DIFF | Transmitter differential return loss | - | - | 0 < -20dB < 100Mhz  100Mhz < -18dB < 300Mhz  300Mhz < -16dB < 600Mhz  600Mhz < -10dB < 2500Mhz  2500Mhz < -9dB < 4875Mhz  4875Mhz < -8dB < 11200Mhz  11200Mhz < -5dB <  16800Mhz  and -3dB beyond that | db |  |
| RLTX-CM | Transmitter common mode return  loss | - | - | 50Hz < -8dB < 15000Mhz | dB |  |
| ZTX\_cal | DC differential TX impedance. Cali-  brated differential driver imped-  ance when in normal mode. | 80 | 100 | 120 | Ω |  |
| T20-80TX | TX Rise/Fall Time | - | - | 0.41 | UI |  |
| TskewTX | TX Differential Skew | 20 | - | 30 | ps |  |
| JTT | Transmitter total jitter (peak-to-  peak) (Tj) | - | - | 65 |  | USB3.0 |
| - | - |  |  | Edp/dp |
| TTX-RJ-PLL | Random jitter (Max) | - | - | 1.4 | Ps rms | USB3.0 and DP is after TXLF |
| TTX-IDLE-TO-DIFF-  DATA | Maximum time to transition to valid  diff signaling after leaving Electrical  Idle | - | - | 8 | ns |  |
| TEIExit | Time to exit Electrical Idle (L0s)  state and to enter L0 | - | - | 5 | Txsys-clk |  |